CASE STUDY

Intel® Xeon® Processor E5 Family
Intel® Xeon® Processor 5650

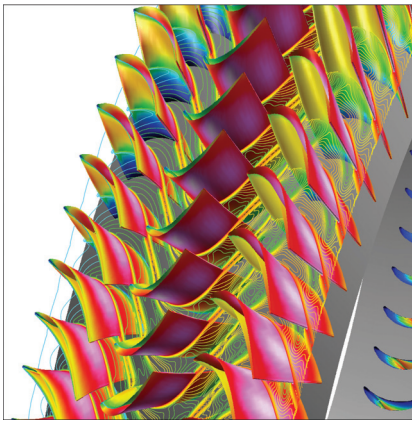
Aerospace and Defense
High-Performance Computing

Parallel Performance for University of Florence and Avio

University turbomachinery research center cuts 260 days from calculation time for complex aeronautical simulations with Intel® Xeon® processors

The University of Florence's Turbomachinery and Energy Systems Research Center (CeRTuS) conducts research into energy conversion, identifying and developing techniques and equipment that can help reduce power consumption. Its focus covers a wide range of disciplines including thermodynamics, physics, mathematical mechanics and fluid dynamics, while taking into account thermal, chemical, plant and economic considerations.

The center has developed a computer code, known as TRAF*, to carry out advanced analysis and research into thermodynamics for the turbomachinery industry. To deliver the best results, such a complex and demanding application needs a high-performance platform to support it, so CeRTuS implemented a code parallelization project on the latest-generation Intel® Xeon® processor E5 family. As a result, it can now complete computations that used to take 265 days in just five.



"We ran numerous benchmarks and the Intel solutions always proved to be the most effective and efficient. In addition to the value of the technology, we also appreciate the assistance of the Intel experts, who work alongside us so proactively."

Andrea Arnone
Director
CeRTuS, University of Florence

CHALLENGES

- **Guarantee performance.** Maintain a competitive advantage over commercial software for the study of fluid dynamics in the aeronautical field
- **Optimize hardware resources.** Take advantage of the potential of next-generation platforms as they arise

SOLUTIONS

- **Code parallelization.** The university initiated a code parallelization project in collaboration with Intel's Software and Services Group
- **A phased approach.** A thorough benchmark resulted in a fruitful collaboration with Intel, enabling gradual introduction of parallelization while partially preserving existing code
- **Hybrid parallelization.** Parallelization was introduced using both the OpenMP* and MPI* standards, creating a very high-performance and flexible hybrid solution

IMPACT

- **Reduced processing time.** Calculations carried out for Avio, which initially required 265 days, were cut to 8.5 days and then just five days with the Intel Xeon processor E5 family[1]
- **Optimization at all levels.** Such a dramatic reduction in processing allows CeRTuS to construct increasingly accurate, complex models and perform more simulations

Thinking ahead

Numerous turbomachinery companies use the TRAF, code which CeRTuS created, working in collaboration with each other and the university. The community of researchers and product developers work together to apply solid academic insights to creating new technologies.

Initiated almost two decades ago, the TRAF project continues to offer a strong advantage over comparable commercial software. "Our added value," says Prof. Andrea Arnone, director of the CeRTuS Research Center of the University of Florence, "is that we have a long-term focus on scientific issues and follow all developments in technology closely. Indeed, we had already started the first trials related to code parallelization 10 years ago.

"At the time, the existing technological infrastructure was not able to adequately support the theoretical premises at the basis of parallelization. However, the latest technology hosts an increasing number of processors within each node, allowing us to move from theory to practice. This is why we decided to begin a code parallelization project now."

Research teams from academia and industry collaborate to drive innovations with enhanced code parallelization

Spotlight on University of Florence

The University of Florence (Università degli Studi di Firenze, UNIFI) is one of Italy's largest and oldest universities, having evolved from the Studium Generale, which was founded by the Florentine Republic in 1321. Its 12 faculties cover areas of study ranging from agriculture to engineering, and it currently has a student population of around 60,000.

A gradual approach

The center faced a number of options for carrying out its code parallelization initiative. First, it needed to choose a technology platform to support it. After running numerous benchmarks, CeRTuS chose a solution powered by the then-latest-generation Intel® Xeon® processor 5650.

After consulting with software optimization experts from Intel's Software and Services Group (SSG), the group responsible for the TRAF project decided to adopt a gradual approach aimed at preserving some of the existing code.

The first step was to optimize the original code. "Using Intel tools and Fortran compiler capabilities, we profiled the code thoroughly and optimized it to obtain the first results," recalls Michele Marconcini, project manager. "Even in the first run, we improved the performance of the computing system by 70 percent[1]."

After this, the team needed to make a choice. It could enter simple compiling instructions and keep the code almost unchanged, a choice that required little time and resources but would eventually come up against the physical limits of even the most powerful infrastructure. Alternatively, the team could intervene in the code in a more invasive way by introducing a more sophisticated parallelism that would allow for the distribution of a calculation across an indefinite number of nodes connected by network cards.

After meticulously examining the pros and cons of both approaches with Intel experts, the TRAF team decided the best strategy was to produce a type of hybrid parallelization, able to operate well on both an individual multi-core machine and a more complex cluster. Once this choice had been made, the standard of reference for the first type of parallelization was created using OpenMP* (an open-source specification for parallel programming) and the Message Passing Interface* (MPI*) standard, which allows for interaction between different calculation nodes.

Concrete results

After experimental trials, the first practical application of the new parallelized code involved computing the aerodynamics of an entire turbine for Avio, an aerospace company with which the University of Florence has been collaborating for 15 years.

Before code parallelization, this process would have taken 265 days. However, by introducing serial optimization and OpenMP parallelization to allow the use of all the cores within a single computing node, the TRAF group, using a server equipped with the Intel Xeon processor 5650 with 12 cores, completed the task in just 33 days.

Introducing two levels of parallelism allows calculations to be divided onto single nodes across a cluster of eight servers equipped, in total, with 96 Intel Xeon processors 5650. This allowed the Avio calculation to be reduced even further – to just 8.5 days.

"Following the introduction of the new Intel Xeon processors E5-2680," said Marconcini, "a trial on a cluster made available by Intel showed that a calculation of this type was completed in just five days. Various enhanced features of the new family of processors (such as use of the cache, registry management, vectorization, data alignment and threading tools) make it considerably more effective, versatile and powerful. Of course, the benefits it offers can be best exploited by using a code such as TRAF, which adopts extreme parallelization."

Besides enjoying faster computations, the center has found that being able to complete more research faster gives it the headroom to create more and increasingly complex models and simulations, with more accurate results. The support provided by the Intel Software and Services Group in this code optimization activity has been fundamental to investigate new software technology and help translate innovation into a real competitive advantage for the CeRTuS University research group.

Marconcini concludes: "For our part, we have already decided that when the time comes to upgrade our infrastructure, probably within a few months, we will definitely adopt the new Intel Xeon processor E5 family."

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[1] Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations, and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products.

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